WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a drain layer having a first conductivity type;

a first drift layer having the first conductivity type and formed on the drain layer;

second drift layers having the first conductivity type and RESURF layers having a second conductivity type, which are formed on the first drift layer and periodically arranged in a direction perpendicular to a direction of depth, the RESURF layer forming a depletion layer in the second drift layer by a p-n junction including the second drift layer and RESURF layer, and the first drift layer having an impurity concentration different from that in the second drift layer;

a drain electrode electrically connected to the drain layer;

a base layer having the second conductivity type and selectively formed in surface regions of the second drift layer and RESURF layer;

a source layer having the first conductivity type and selectively formed in a surface region of the base layer;

a source electrode formed in contact with surfaces of the base layer and source layer; and

a gate electrode formed on the base layer located between the source layer and the second drift layer

with a gate insulating film interposed therebetween.

2. The device according to claim 1, wherein the impurity concentration in the first drift layer is lower than that in the second drift layer.

3. The device according to claim 2, wherein a ratio of a thickness of the second drift layer to a sum of thicknesses of the first and second drift layers falls within a range of 0.21 to 0.8.

4. The device according to claim 2, wherein an impurity amount contained in the RESURF layer falls within a range of 0.87 to 1.5 times that contained in the second drift layer.

5. The device according to claim 2, wherein a depth of the RESURF layer falls within a range of 0.95 to 1.05 times that of the second drift layer.

6. The device according to claim 5, wherein an impurity amount contained in the RESURF layer falls within a range of 1 to 1.3 times that contained in the second drift layer.

7. The device according to claim 2, wherein when a rated voltage is applied between the source and drain electrodes, the RESURF layer and base layer completely deplete the second drift layer by at least one of the p-n junction including the second drift layer and RESURF layer and a p-n junction including the second drift layer and base layer.

8. The device according to claim 2, wherein when

a voltage not less than 1/2 a rated voltage is applied between the source and drain electrodes, the RESURF layer and base layer completely deplete the second drift layer by at least one of the p-n junction including the second drift layer and RESURF layer and a p-n junction including the second drift layer and base layer.

9. The device according to claim 2, wherein at least one of the second drift layer and RESURF layer has an impurity concentration profile in which the impurity concentration changes in the direction of depth.

10. The device according to claim 2, further comprising a first insulating film formed between the second drift layer and the RESURF layer.

11. The device according to claim 2, further comprising a first insulating film formed in one of the second drift layer and RESURF layer.

12. The device according to claim 10, wherein at least one of the second drift layer and RESURF layer has an impurity concentration profile in which the impurity concentration changes in the direction perpendicular to the direction of depth.

13. The device according to claim 2, wherein the second drift layer and RESURF layer are formed even on the first drift layer at an element terminating portion in the same manner as that at an element central

portion.

14. The device according to claim 2, further comprising a first semiconductor layer having the first conductivity type, which is formed on the first drift layer at an element terminating portion and has an impurity concentration lower than that in the second drift layer.

15. The device according to claim 2, wherein the first drift layer has an impurity concentration profile in which the impurity concentration changes in the direction of depth.

16. The device according to claim 2, further comprising a plurality of second semiconductor layers having the first conductivity type, which are formed at a lower portion of the first drift layer at a predetermined interval and have an impurity concentration higher than that in the first drift layer.

17. The device according to claim 1, wherein the second drift layers and RESURF layers are formed to fill a plurality of first trenches formed in the first drift layer, and the RESURF layers sandwich the second drift layers in the direction perpendicular to the direction of depth, and each RESURF layer has one side wall in contact with the first drift layer and the other side wall in contact with the second drift layer.

18. The device according to claim 17, wherein a width of the first drift layer located between adjacent

first trenches is different from that of the second drift layer adjacent to the first drift layer via the RESURF layer.

19. The device according to claim 17, further comprising:

a third semiconductor layer having the second conductivity type and formed on a side wall of a second trench formed in the first drift layer at an element terminating portion;

a fourth semiconductor layer having the first conductivity type, which is formed to fill the second trench and sandwiched between the third semiconductor layers in the direction perpendicular to the direction of depth; and

a fifth semiconductor layer having the second conductivity type, which is formed in a surface region of the fourth semiconductor layer to electrically connect a plurality of third semiconductor layers.

20. The device according to claim 19, wherein

the fifth semiconductor layer is electrically connected to the base layer, and

at least one of a p-n junction including the third and fourth semiconductor layers and a p-n junction including the fourth and fifth semiconductor layers forms a depletion layer in the fourth semiconductor layer.

21. The device according to claim 17, further

comprising:

a sixth semiconductor layer having the second conductivity type, which is formed on a bottom surface and side walls of a third trench formed in the first drift layer at an element terminating portion;

a seventh semiconductor layer having the first conductivity type, which is formed on the sixth semiconductor layer to fill the third trench; and

an eighth semiconductor layer having the second conductivity type, which is formed in a surface region of the seventh semiconductor layer to surround the seventh semiconductor layer together with the sixth semiconductor layer.

22. The device according to claim 21, wherein the eighth semiconductor layer electrically connects a plurality of seventh semiconductor layers.

23. The device according to claim 21, wherein

the eighth semiconductor layer is electrically connected to the base layer, and

at least one of a p-n junction including the sixth and seventh semiconductor layers and a p-n junction including the seventh and eighth semiconductor layers forms a depletion layer in the seventh semiconductor layer.

24. The device according to claim 17, further comprising:

a ninth semiconductor layer having the second

conductivity type and formed at least on a side wall of a fourth trench formed in the first drift layer at an element terminating portion;

a 10th semiconductor layer having the first conductivity type, which is formed to fill the fourth trench and located in the fourth trench while being sandwiched between the ninth semiconductor layers in the direction perpendicular to the direction of depth;

a second insulating film formed on the ninth and 10th semiconductor layers; and

one of metal layer and 11th semiconductor layers formed on the second insulating film, the 11th semiconductor layer made of a conductive material.

25. The device according to claim 1, further comprising one of a third insulating film and 12th semiconductor layer formed in the RESURF layer, the 12th semiconductor layer having an impurity concentration lower than those in the second drift layer and RESURF layer,

wherein the RESURF layer is located between the second drift layer and one of the third insulating film and 12th semiconductor layer.

26. The device according to claim 1, further comprising one of a third insulating film and 12th semiconductor layer formed in the second drift layer, the 12th semiconductor layer having an impurity concentration lower than those in the second drift

layer and RESURF layer,

wherein the second drift layer is located between the RESURF layer and one of the third insulating film and 12th semiconductor layer.

27. A semiconductor device comprising:

a drain layer having a first conductivity type;

a drift layer having the first conductivity type, which is formed on the drain layer and has an impurity concentration lower than that in the drain layer; and

a RESURF layer having a second conductivity type and formed to extend from a surface of the drift layer into the drain layer, the RESURF layer forming a superjunction structure together with the drift layer and forming a depletion layer in the drift layer.

28. The device according to claim 27, further comprising one of a first insulating film and first semiconductor layer formed to extend from a surface of the RESURF layer to the drain layer, the first semiconductor layer having an impurity concentration lower than those in the drift layer and RESURF layer,

wherein the RESURF layer is located between the drift layer and one of the first insulating film and first semiconductor layer.

29. The device according to claim 28, wherein the RESURF layer is located between the drain layer and one of the first insulating film and first semiconductor layer and between the drift layer and one of the first

insulating film and first semiconductor layer.

30. The device according to claim 28, further comprising:

a base layer having the second conductivity type and formed in surface regions of the drift layer and RESURF layer;

a source layer having the first conductivity type and formed in a surface region of the base layer; and

a gate electrode formed on the base layer between the drift layer and the source layer with a gate insulating film interposed therebetween.

31. The device according to claim 30, further comprising a second semiconductor layer having the first conductivity type, which is formed between the RESURF layer and the drain layer and between the RESURF layer and the drift layer and has an impurity concentration higher than that in the drift layer.

32. The device according to claim 30, wherein a bottom surface of the RESURF layer is located at a position deeper than a bottom surface of the drift layer.

33. The device according to claim 30, wherein

the RESURF layer has a planar pattern with a stripe shape in a first direction along the gate electrode in an element region where a semiconductor element is present,

a plurality of RESURF layers are formed at

an element terminating portion in a second direction perpendicular to the first direction, and

the plurality of RESURF layers at the element terminating portion are electrically connected.

34. The device according to claim 33, further comprising one of a conductive film and third semiconductor layer formed on the RESURF layer and drift layer to connect the plurality of RESURF layers at the element terminating portion.

35. The device according to claim 34, wherein an upper portion of one of the first insulating film and first semiconductor layer at the element terminating portion is recessed, and the recessed region is further filled with the RESURF layer.

36. The device according to claim 30, wherein

the RESURF layer has a planar pattern with a stripe shape in a first direction along the gate electrode in an element region where a semiconductor element is present,

a plurality of RESURF layers are formed at an element terminating portion in a second direction perpendicular to the first direction, and

the RESURF layers at the element terminating portion have a planar pattern with a stripe shape along the second direction.

37. The device according to claim 30, wherein the RESURF layers are arranged in a matrix.

38. The device according to claim 30, further comprising a fourth semiconductor layer formed between the RESURF layer and one of the first insulating film and first semiconductor layer,

wherein the base layer is formed in surface regions of the drift layer, RESURF layer, and fourth semiconductor layer.

39. The device according to claim 38, further comprising a fifth semiconductor layer having the first conductivity type, which is formed between the RESURF layer and the drift layer and has an impurity concentration higher than that in the drift layer.

40. The device according to claim 38, wherein the fourth semiconductor layer has an impurity concentration lower than those in the drift layer and RESURF layer.

41. The device according to claim 38, wherein the fourth semiconductor layer has an impurity concentration almost equal to that in one of the drift layer and RESURF layer and the same conductivity type as that of the drift layer.

42. The device according to claim 27, further comprising one of a first insulating film and first semiconductor layer formed to extend from a surface of the drift layer to the drain layer, the first semiconductor layer having an impurity concentration lower than those in the drift layer and RESURF layer,

wherein the drift layer is located between the RESURF layer and one of the first insulating film and first semiconductor layer.

43. The device according to claim 42, wherein the drift layer is located between the drain layer and one of the first insulating film and first semiconductor layer and between the RESURF layer and one of the first insulating film and first semiconductor layer.

44. The device according to claim 42, further comprising:

a base layer having the second conductivity type and formed in surface regions of the drift layer and RESURF layer;

a source layer having the first conductivity type and formed in a surface region of the base layer; and

a gate electrode formed on the base layer between the drift layer and the source layer with a gate insulating film interposed therebetween.

45. The device according to claim 44, wherein

the drift layer has a planar pattern with a stripe shape in a first direction along the gate electrode in an element region where a semiconductor element is present,

at an element terminating portion, the RESURF layer is formed on the drain layer,

a plurality of drift layers are formed in the RESURF layers at the element terminating portion in

a second direction perpendicular to the first direction, and

the plurality of RESURF layers at the element terminating portion are electrically connected.

46. The device according to claim 45, further comprising one of a conductive film and second semiconductor layer formed on the RESURF layer and drift layer to connect the plurality of RESURF layers at the element terminating portion.

47. The device according to claim 46, wherein an upper portion of one of the first insulating film and first semiconductor layer at the element terminating portion is recessed, and the recessed region is further filled with the drift layer.

48. The device according to claim 44, wherein

at an element terminating portion, the RESURF layer is formed on the drain layer,

the drift layer has a planar pattern with a stripe shape in a first direction along the gate electrode in an element region where a semiconductor element is present,

a plurality of drift layers are formed at the element terminating portion in a second direction perpendicular to the first direction, and

the drift layers at the element terminating portion have a planar pattern with a stripe shape along the second direction.

49. The device according to claim 44, wherein the drift layers are arranged in a matrix.

50. The device according to claim 44, further comprising a third semiconductor layer formed between the drift layer and one of the first insulating film and first semiconductor layer,

wherein the base layer is formed in surfaces of the drift layer, RESURF layer, and third semiconductor layer.

51. The device according to claim 50, wherein the third semiconductor layer has an impurity concentration lower than those in the drift layer and RESURF layer.

52. The device according to claim 50, wherein the third semiconductor layer has an impurity concentration almost equal to that in one of the drift layer and RESURF layer and the same conductivity type as that of the drift layer.

53. The device according to claim 44, wherein a bottom surface of the drift layer is located at a position deeper than a bottom surface of the RESURF layer.

54. A method for fabricating a semiconductor device, comprising:

forming a first drift layer having a first conductivity type on a drain layer having the first conductivity type;

forming a trench in a surface region of the first

drift layer;

forming a first RESURF layer having a second conductivity type by doping an impurity into an inner wall side surface of the trench;

forming a second drift layer having the first conductivity type in the trench;

selectively forming a base layer having the second conductivity type in surface regions of the first and second drift layers and first RESURF layer;

selectively forming a source layer having the first conductivity type in a surface region of the base layer;

forming a gate insulating film on the base layer located at least between the first drift layer and the source layer and between the second drift layer and the source layer; and

forming a gate electrode on the gate insulating film.

55. The method according to claim 54, wherein formation of the second drift layer is stopped before the second drift layer completely fills the trench, and

the method further comprises, after formation of the second drift layer is stopped, forming an insulating film on the second drift layer so as to fill a remaining portion in the trench.

56. The method according to claim 54, wherein formation of the second drift layer is stopped before

the second drift layer completely fills the trench, and

the method further comprises, after formation of the second drift layer is stopped, moving atoms in the second drift layer by annealing in an atmosphere containing hydrogen so as to fill a remaining portion in the trench.

57. The method according to claim 54, wherein formation of the second drift layer is stopped before the second drift layer completely fills the trench, and

the method further comprises, after formation of the second drift layer is stopped, doping an impurity into a surface of the second drift layer exposed into the trench so as to form a second RESURF layer having the second conductivity type, and

forming a third drift layer having the first conductivity type in the trench so as to fill the trench.

58. The method according to claim 54, wherein forming the first RESURF layer includes ion-implanting the impurity in an oblique direction with respect to a direction of depth of the trench.

59. A method for fabricating a semiconductor device, comprising:

forming a first drift layer having a first conductivity type on a drain layer having the first conductivity type;

forming a trench in a surface region of the first

drift layer;

forming a RESURF layer having a second conductivity type by doping an impurity into a side surface of the trench;

forming a second drift layer having the first conductivity type by doping an impurity into a surface of the RESURF layer exposed into the trench;

moving atoms in the second drift layer by annealing in an atmosphere containing hydrogen so as to fill a remaining portion in the trench;

selectively forming a base layer having the second conductivity type in surface regions of the first and second drift layers and RESURF layer;

selectively forming a source layer having the first conductivity type in a surface region of the base layer;

forming a gate insulating film on the base layer located at least between the first drift layer and the source layer and between the second drift layer and the source layer; and

forming a gate electrode on the gate insulating film.

60. The method according to claim 59, wherein in forming the RESURF layer, the RESURF layer is formed by ion-implanting the impurity from an oblique direction with respect to a direction of depth of the trench.

61. A method for fabricating a semiconductor

device, comprising:

forming a drift layer having a first conductivity type on a drain layer having the first conductivity type, the drift layer having an impurity concentration lower than that in the drain layer;

forming a trench extending from a surface of the drift layer into the drain layer;

forming a RESURF layer having a second conductivity type in the trench;

selectively forming a base layer having the second conductivity type in surface regions of the drift layer and RESURF layer;

selectively forming a source layer having the first conductivity type in a surface region of the base layer;

forming a gate insulating film on the base layer located at least between the drift layer and the source layer; and

forming a gate electrode on the gate insulating film.

62. The method according to claim 61, wherein forming the RESURF layer includes:

forming the RESURF layer along side and bottom surfaces of the trench so as not to completely fill the trench; and

forming, on the RESURF layer, one of a first semiconductor layer and insulating film to fill the

trench, the first semiconductor layer having an impurity concentration lower than those in the drift layer and RESURF layer.

63. The method according to claim 61, wherein forming the RESURF layer includes ion-implanting an impurity from the trench into the drift layer from an oblique direction to form the RESURF layer on a side wall of the trench.

64. The method according to claim 63, further comprising, after the RESURF layer is formed, forming, in the trench, one of a first semiconductor layer and insulating film to fill the trench, the first semiconductor layer having an impurity concentration lower than those in the drift layer and RESURF layer.

65. The method according to claim 61, wherein

in forming the trench, a plurality of trenches having a planar pattern with a stripe shape are formed,

in forming the gate electrode, the gate electrode is formed into a planar pattern with a stripe shape along the same direction as that of the trenches, and

forming the RESURF layer includes:

forming the RESURF layer on the drain layer and drift layer so as not to completely fill the trench;

forming, on the RESURF layer, one of a first semiconductor layer and insulating film so as to completely fill the trench, the first semiconductor layer having an impurity concentration lower than those

in the drift layer and RESURF layer; and

removing and planarizing one of the insulating film and first semiconductor layer and part of the RESURF layer until the drift layer is exposed.

66. The method according to claim 65, further comprising after forming the trench, forming, on the drain layer and drift layer, a second semiconductor layer having the first conductivity type and an impurity concentration higher than that in the drift layer so as not to completely fill the trench,

wherein the RESURF layer is formed on the second semiconductor layer.

67. The method according to claim 61, wherein

in forming the trench, a plurality of trenches having a planar pattern with a stripe shape are formed,

in forming the gate electrode, the gate electrode is formed into a planar pattern with a stripe shape along the same direction as that of the trenches, and

forming the RESURF layer includes:

forming the RESURF layer having the second conductivity type by ion-implanting, from an oblique direction, an impurity into the drift layer exposed to a side wall of the trench;

forming, on the drain layer, drift layer, and RESURF layer, a third semiconductor layer having an impurity concentration lower than those in the drift layer and RESURF layer so as not to completely fill

the trench;

forming, on the third semiconductor layer, one of a fourth semiconductor layer and insulating film so as to completely fill the trench, the fourth semiconductor layer having an impurity concentration lower than those in the drain layer, drift layer, and RESURF layer; and

removing and planarizing one of the insulating film and fourth semiconductor layer and part of the third semiconductor layer until the drift layer is exposed.

68. The method according to claim 61, wherein in the step of forming the RESURF layer, the RESURF layer is formed in an element region where a semiconductor element is to be formed, and at an element terminating portion to surround the element region.

69. The method according to claim 61, wherein in the step of forming the trench, the trench is formed in an element region where a semiconductor element is to be formed, and at an element terminating portion in a second direction perpendicular to a first direction along the gate electrode.

70. The method according to claim 69, wherein in the step of forming the trench, the trench at the element terminating portion is formed to have a stripe pattern along the second direction.

71. The method according to claim 69, wherein in the step of forming the trench, the trench at the

element terminating portion is formed and arranged in a matrix.